REMARKS

Applicants thank the Examiner for acknowledging receipt of Applicants' foreign priority document, Japanese Application No. 2000-290259, that has been submitted pursuant to 35 U.S.C. section 119. Applicants also thank the Examiner for recognizing the patentable distinctions over Abdelgadir, Patent No. 6,274,933, and that the 35 U.S.C. § 112 rejections relating to the "at least 10%" claim language were not proper.

Applicants respectfully request reconsideration of the prior art rejection of Claims 1-3 set forth by the Examiner under 35 U.S.C. § 102. Applicants respectfully submit that the prior art references of record whether considered alone, or in combination, fail to either teach or suggest Applicants' presently claimed invention.

Applicants note that the *Jang*, Patent No. 6,180,540, teaches the application of Chemical Mechanical Polishing (CMP) to the Fluorine-doped Silicon layer immediately after deposition. The CMP process reacts directly with the Fluorinated Silicate Glass (FSG) layer and creates a "hydrated" SiF layer. (Col. 6, lns 40-59). *Jang* then applies a plasma etch to remove the hydrated SiF layer before optionally applying a dielectric layer "cap." (Col. 7, lns 13-19; Col. 8 lns 3-15). In contrast, Applicant's invention, notably employs the use of sputtering to remove a surface layer of the SiF deposition, followed by the deposition of a 2nd dielectric-layer composed of P-TEOS to further insulate the SiF layer. Applicants avoid the necessity of removing the hydrated SiF layer by not applying a CMP process directly to the SiF layer. Because these processes are significantly different, a §102 rejection cannot be

sustained. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of* California, 814 F.2d 628, 631 (Fed. Cir. 1987). Therefore, Examiner's claim that *Jang* stands as a valid 35 U.S.C. § 102 rejection is not supported, and Claims 1-3 should be allowed. Applicant has also added new claim 6 to further underscore these distinctions.

Applicants respectfully request reconsideration of the obviousness rejection of Claims 4-5 set forth by the Examiner under 35 U.S.C. § 103 in light of the following remarks. The Examiner's rejection is based on hindsight, and as such, does not properly support an obviousness rejection. The US Court of Appeals for the Federal Circuit has held that "combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability." *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999).

Applicants' claimed invention is directed to improved methods for manufacturing semiconductor devices. More specifically, Applicants' claimed invention is directed to a method for producing a semiconductor device having a fluorine-doped silicon oxide layer as well as a second silicon oxide layer formed over the fluorine-doped silicon oxide layer. Advantageously, Applicants have discovered that significant improvements over prior art techniques can be achieved by additionally and selectively removing a surface layer of the fluorine-doped silicon oxide layer by sputtering. For example, the Specification discloses that about 100 nm of the surface layer of the FSG layer 13 is removed after the formation of

the FSG layer 13 and prior to formation of the insulating layer. See page 11, lines 29-32. Subsequently, the silicon oxide layer is formed after the formation of the FSG layer. See generally page 12, lines 8-13.

Applicants note that the new prior art cited by the Examiner, *Rana et al* U.S. Patent No. 6,191,026, is directed to an apparatus for filling voids in semiconductors. The invention in *Rana* is directed to a totally different process and objective than applicants, and thus, cannot satisfy the teaching requirement of *In re Dembiczak*. *Rana* teaches etching the corners of a void, which is a defect in the semiconductor chip, in order to make the subsequent filling of the void by Chemical Vapor Deposition of fluorine-doped silicate glass (FSG) easier. The fact that *Rana* uses Fluorine doped Silicon as an interlayer dielectric and uses a sputter etchback method at some point in the process, as applicants' invention also uses at some point, does not provide any suggestion or teaching to apply *Rana* to applicants' inventive method in a 35 U.S.C. § 103 rejection. Further, Examiner states at the bottom of page 3 in the Response to Arguments section that "Examiner agrees with the applicant's argument that *Abdelgadir et al* does not disclose an additional step of removing a surface layer of the FSG." Therefore, after *Rana* and *Abdelgadir* are removed, only *Jang* remains in Examiner's §103 rejection at the top of page 3. And since *Jang* (6,180,540) alone does not teach applicant's invention, claims 4-5 should now be allowed.

Applicants further note that *Rana* is not a proper reference because it is non-analogous art in that it is directed to the repair of a defect in a semiconductor and does not

provide teaching or suggestion concerning improvements in original manufacturing techniques. New claims have also been added to further underscore the distinctions.

Accordingly, Applicants' invention is patentability distinct over the art of record. In light of the foregoing, Applicants respectfully submit that all claims now stand in condition for allowance.

Respectfully submitted,

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